SMARTEYE P-Linc

Application Interface Package for the Allen Bradley PLC-5

Application Note - SA0034

Revision 1

Prepared by:

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2637 Bond Street
Rochester Hills, MI 48309

Revision 1, June 27, 1996

related documents:

SMARTEYE P-Linc User Manual

This document was produced using Microsoft® Word

Printed in U.S.A.

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1.0 Introduction

The Smarteye P-Linc connects up to 8 Smarteye Electronic Assemblies: (SEA-8s and/or Twins) on a serial RS485 multidrop communication line. Smarteye reader data is received on the serial communication line and converted to parallel digital 24VDC outputs. The digital outputs of the P-Linc are directly wired to digital input modules of a PLC. Two bits of the output data, the data ready bits, signal the preparation of new data on the output lines. A control device recognizes new data, receives it, and then provides two output bits which match the data ready bits. These outputs are received by the P-Linc on its two 24VDC input lines and interpreted as data acknowledge bits.

The P-Linc parallel port has 28 bits: 26 outputs and 2 inputs. The 26 outputs consist of: 16 data bits, 6 reader bits, 2 data ready bits, a parity bit and a label or error bit. The two input bits are used for data acknowledge. The 16 data bits and 6 reader bits can be configured as either binary or BCD.

2.0 Parallel Wiring

The P-Linc circuit card provides plug-in screw terminals for the 26 parallel output and 2 parallel input connections. Discrete 18 gauge wire such as Belden 8501 or equivalent is recommended for these connections. Parallel wiring details can be found on drawing #SP2004/01-411 in Appendix 'A'.

Notes:

1. Data presented by a P-Linc on its parallel output lines is binary; i.e., each output represents a bit in a binary field (off = 0, on =1).
2. The least significant bit of the data field is D0 and the most significant is D15. The least significant bit of the reader field is RDR0 and the most significant is RDR5.
3. Connecting all P-Linc parallel outputs to an input module may not be necessary. Example: binary mode with 10 bit labels, D0 - D9 must be wired, D10 - D15 will always be 0 and wiring is therefore optional.
4. The P-Linc is configured for true-high operation; i.e., a binary 1=24VDC and a binary 0=GND.

2.1 Data Bits (D0-D15)

The data bits (D0 - D15) define the value of the label or error number. This field may be binary or BCD dependent on the position of SW2.1. (Please refer to the P-Linc User Manual for additional information on dip switch configuration.)

2.2 Reader Bits (RDR0 - RDR5)

The reader bits (RDR0 - RDR5) define the value of the reader number. This field may be binary or BCD dependent on the position of SW2.1.

2.3 Ready Bits (RDY0, RDY1)

A change of state in the two ready bits signals the control device that the P-Linc has new data on its output lines. If the ready bits are 01 or 10, then the control device should receive the new data and perform appropriate control action. If the ready bits are 00 or 11, then the control device should ignore the data (take no control action). A full description of this protocol appears in section 4. - 'Parallel Communication Protocol'.

2.4 Parity Bit (PARITY)

The parity bit enables the control device to determine the validity of data received from the P-Linc. Thus, if an input/output point should fail on either the control device or the P-Linc, or if a connection between the two should be lost, then the control device can detect the fault and issue an alarm and/or stop the controlled operation until repairs are made.

The value of the parity bit is always set so that an **odd** sum results when the number of bits turned on in the data field (D0-D15), the reader field (RDR0-RDR5), and the Label/Error bit (L/E), are added with the parity bit itself.

2.5 Label/Error Bit (L/E)

The label or error (L/E) bit defines the data bits (D0 - D15) as an error number or a label number. **If this bit is a 1, the data is a label number. If the bit is a 0, the data is an error number.**

2.6 Data Acknowledge (ACK0, ACK1)

The two data acknowledge bits are the only parallel **inputs** received by the P-Linc. A control device must set the data acknowledge bits to the **same** value as the two data ready bits, signaling recognition of the most recent transition of data ready. A full description of this protocol appears in section 4. - 'Parallel Communication Protocol'.

3.0 Power-Up

When power is applied an LED on the power supply will illuminate. The P-Linc reads its setup switches and initializes its internal data. The control port transmit LED will begin to flash and the receive LED will flash if the control port is wired properly to one or more SEA units. One of the parallel port RDY bit LEDs will illuminate when valid data is on the parallel port.

4.0 Parallel Communication Protocol

The communication protocol between a P-Linc and a control device (e.g., programmable controller) is relatively simple. Nevertheless, it is important that a logic designer for the control device be thoroughly familiar with the protocol.

4.1 Transaction Steps

All data messages originate at an SEA unit. A set of messages in both directions is required for an SEA unit to deliver the data to the P-Linc and receive assurance of its delivery. The complete set of messages between an SEA Unit and the P-Linc, as well as the P-Linc and the PLC, is a data message transaction. The key steps of a data message transaction include the following:

1. The P-Linc selects the next SEA unit to poll from its on line list and sends a box poll command to that SEA unit.
2. The SEA unit responds with a data message.
3. The P-Linc sends a brief message back to the SEA unit, acknowledging receipt of the data message.
4. The P-Linc extracts data from the serial data message and establishes it on the parallel port.
5. Once the data has settled on the data lines the P-Linc will establish a new state for the data ready bits and write this new state to RDY0 and RDY1 of the parallel output lines.
6. Meanwhile, the PLC which has been monitoring the data ready outputs of the P-Linc, recognizes the change in the data ready bits.

   If the data ready bits are 01 or 10, then the PLC receives the remainder of the data from the parallel outputs and takes appropriate action.

   Whatever the new pattern of data ready bits, the control device sets data acknowledge bits to match.
7. When the P-Linc receives ACK0 and ACK1 equal to RDY0 and RDY1, then the transaction is complete.

4.2 Design Considerations

A P-Linc, regardless of the speed of its output buffers, cannot guarantee that all new output data will transition at the same instant. In other words, there is a short transient interval during which output data 'settles'. A PLC samples data presented by a P-Linc at scattered instances in time, including an instant during which the output lines of a P-Linc are settling.

The steps of a data message transaction are designed to prevent a control device from receiving data that is sampled during a settling period. In order to prevent this, the transaction steps allow output data to settle before the data ready bits change. Thus, a control device should only receive data when it recognizes a change in the data ready bits.

There are four possible patterns of the two data ready bits: 00, 01, 10, and 11. Only 01 and 10 are associated with usable data. Thus, a control device should receive data only when the data ready bits change and have a value of 01 or 10. This prevents a receipt of data during a settling period of the data ready bits, when 00 and 11 are possible values.

There is only one instance in which data ready is deliberately set (non-transient) to a value other than 01 or 10. At powerup, when there is no data yet established for the parallel port the initial value of data ready is 00. The associated parallel data may be ignored by the control device, as with any other instance of 00 for data ready.

A control device should reflect all values of data ready in its data acknowledge outputs, even values of 00 and 11. A P-Linc will not begin a new data message transaction until data ready of the previous transaction is matched by data acknowledge.

5.0 PLC-5 Ladder Logic Explanation

An example program and memory map is included in Appendix B which is described in this section.

The PLC logic begins by buffering the current ready bits in rung 2:0, the data bits are buffered in rung 2:3.

The PLC logic must recognize when the states of the ready bits have changed. This is accomplished by storing the last state of the ready bits and comparing them to the new state. See rung P2:1. If new data is available, then the new state of the ready bits is copied to the last state and the ACK outputs. See rungs P2:37 and P2:38. If new data is not available then the program skips down to rung 2:36.

The parity is calculated by adding the number of bits that are on. The 16 data bits, the 6 reader bits, the parity bit, and the L/E bit are each checked. If the bit is on, a constant value of one is added to the parity sum word. The final result of the parity sum word should be an odd number, or the LSB should be a one. See rung P2/29.

If the parity is ok, the program proceeds to mask off the reader number (2:31), test label numbers for high and low user set limits (2:32), and write the valid label or error to the user data words (2:34 and 2:35). A label ready bit or error ready bit (read event flags) is set when new data is moved into the user data words. The read event flags are intended to be trigger bits. When one of these trigger bits transitions from off to on, this means that a new label or error is now in the user data word. The user program should read the label or error from the user data word and clear the trigger bit so it can be set again for the next label read.

The fault bit is set when the parity test fails, or when a label is read which is larger or smaller than the defined range (2:36).

The integer constant words shown on the PLC memory map drawing must be set up before running the program.

6.0 Appendix 'A' (Drawing)

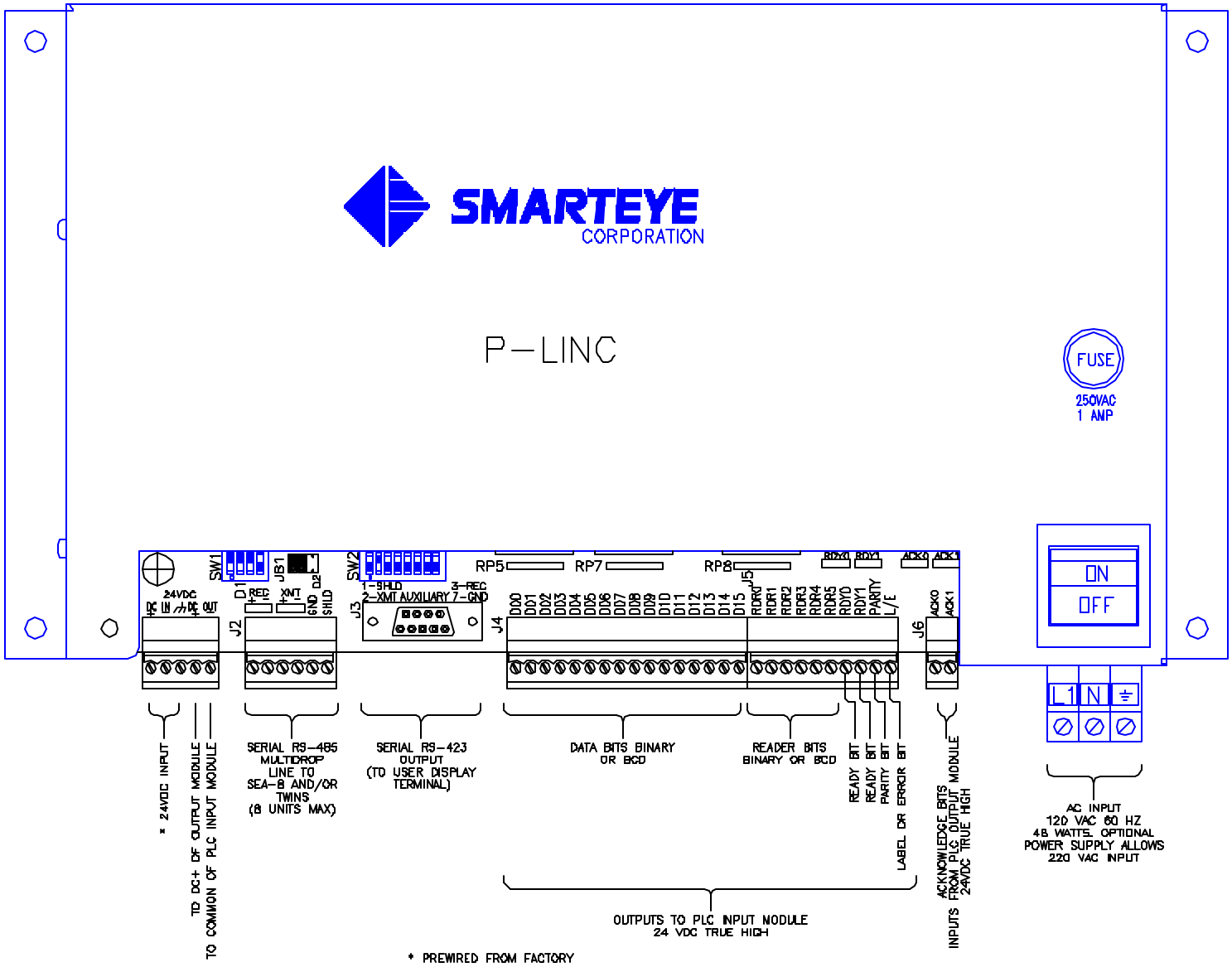
Field Wiring Details – SP2004/01-411

PLC-5 Memory Map for Parallel Interface Application - SA0034-810

REV	DESCRIPTION	DATE	APPR. BY
0	INITIAL RELEASE	10/3/94	MDB

SMARTEYE CORPORATION

P-LINC



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DRAWN BY:	RSA
CHECKED BY:	MDB
ENGINEER:	KLC
DATE:	9/15/94
SHEET	1 OF 1
SCALE:	NTS
SIZE:	D

TITLE: SMARTEYE P-LINC
FIELD WIRING DETAILS

DRAWING NO. SP2004/01-411

H:\SMARTEYE\PRODUCTS\SP2004-1_P-LINC\411-1-D.DWG PLOTTED: 04-02-03 AT 10:26

INPUT WORDS

I:000 — 17 16 15 14 13 12 11 10 7 6 5 4 3 2 1 0 — X X X X X X

I:001 — 17 16 15 14 13 12 11 10 7 6 5 4 3 2 1 0

N101:10 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — X X X X X X

L/E, PARITY, RDY1, RDY0, RDR5, RDR4, RDR3, RDR2, RDR1, RDR0

N101:11 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

OUTPUT WORD FROM OUTPUT MODULE

O:000 — 17 16 15 14 13 12 11 10 7 6 5 4 3 2 1 0 — X X X X X X X X X X X X X X

ACK1, ACK0

INTEGER CONSTANT WORDS

N101:001 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 — SET EQUAL TO 1

N101:002 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 — READER # SET AS SHOWN

N101:003 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — LABEL # LOW LIMIT

N101:004 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — LABEL # HIGH LIMIT

INTEGER APPLICATION WORDS

N101:012 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — X X X X X X X X X X X X — PARITY OK BIT

P-LINC DATA FAULT, LABEL RANGE OK BIT, PARITY OK BIT, NEW DATA AVAIL

N101:013 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — PARITY SUM WORD

N101:014 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — X X X X X X X X X X X X X X X X — ACKNOWLEDGE BITS

N101:015 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — X X X X X X X X X — RDR#

INTEGER USER LABEL WORDS

N102:000 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — RDR 0

N102:001 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — RDR 1

N102:002 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — RDR 2

N102:063 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — RDR 63

B104 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — LABEL READY BITS

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 — LABEL READY BITS

47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 — LABEL READY BITS

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 — LABEL READY BITS

INTEGER USER ERROR WORDS

N103:000 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — RDR 0

N103:001 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — RDR 1

N103:002 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — RDR 2

N103:063 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — RDR 63

B105 — 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — ERROR READY BITS

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 — ERROR READY BITS

47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 — ERROR READY BITS

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 — ERROR READY BITS

REV	DESCRIPTION	DATE	APPR. BY
0	INITIAL RELEASE	6/4/96	J.E.L.
1	MODIFIED MEMORY ADDRESSING		

LEGEND

X – NOT USED

1 – ON

0 – OFF

SMARTEYE CORPORATION

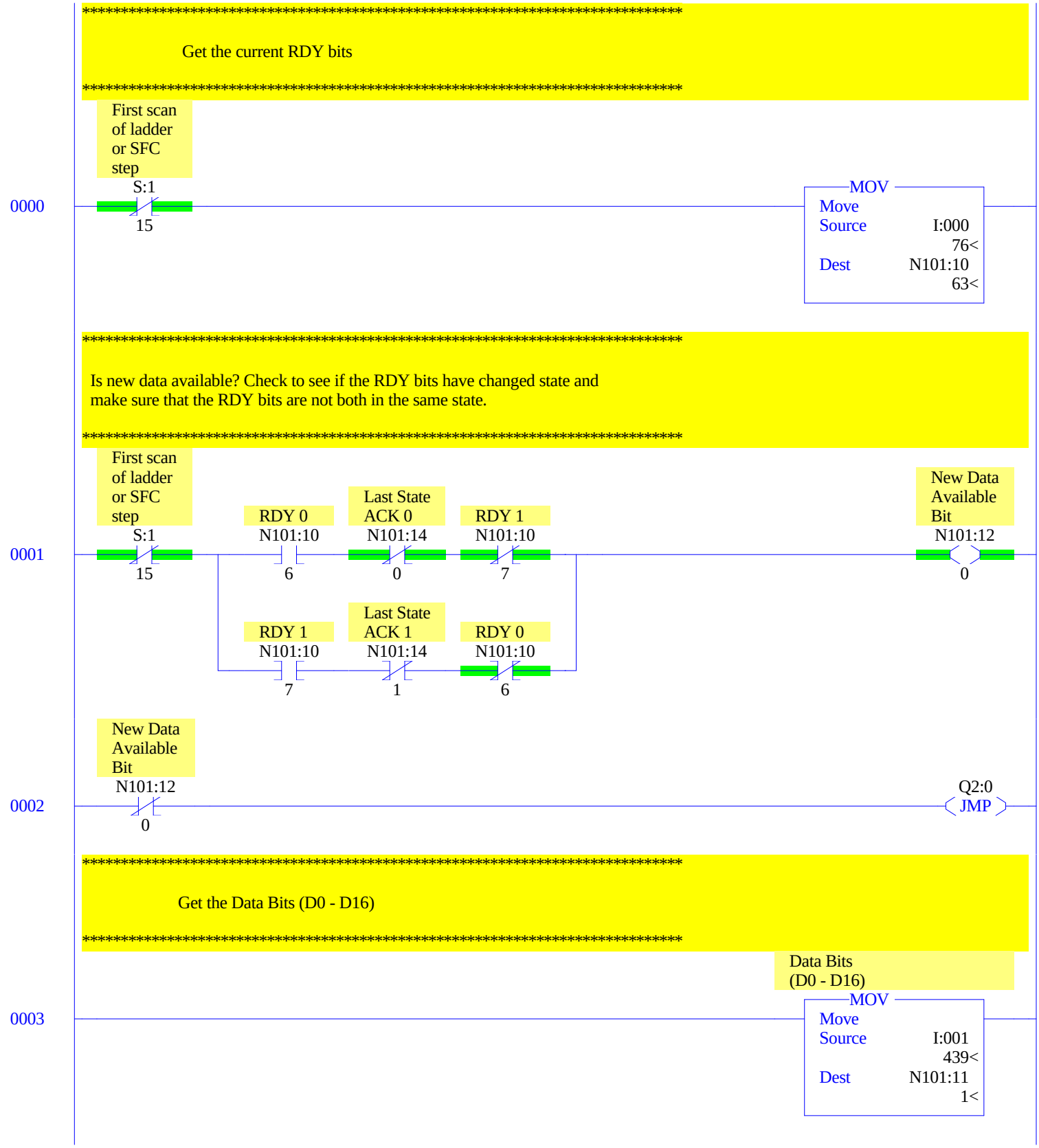
20002 STEPHENSON HWY – TROY, MICHIGAN – 48083

DRAWN BY:	R.S.A.
CHECKED BY:	J.E.L.
ENGINEER:	J.E.L.
DATE:	6/3/96
SHEET NO.	1 OF 1
SCALE:	NONE
SIZE:	D

TITLE: PLC-3 MEMORY MAP FOR P-LINC APPLICATION

DRAWING NO. SA0034-810

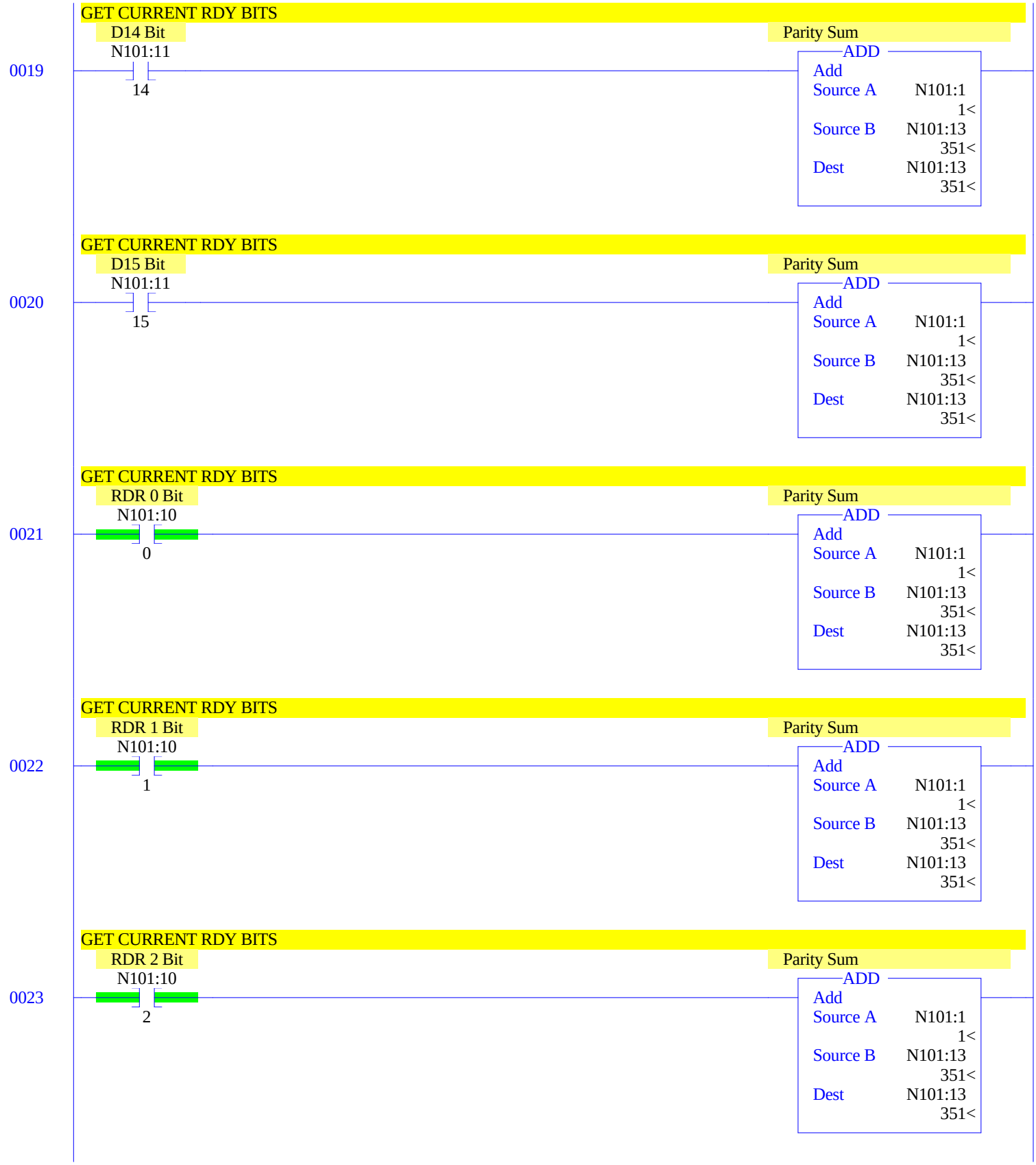
7.0 Appendix 'B' (Example PLC-5 Program)

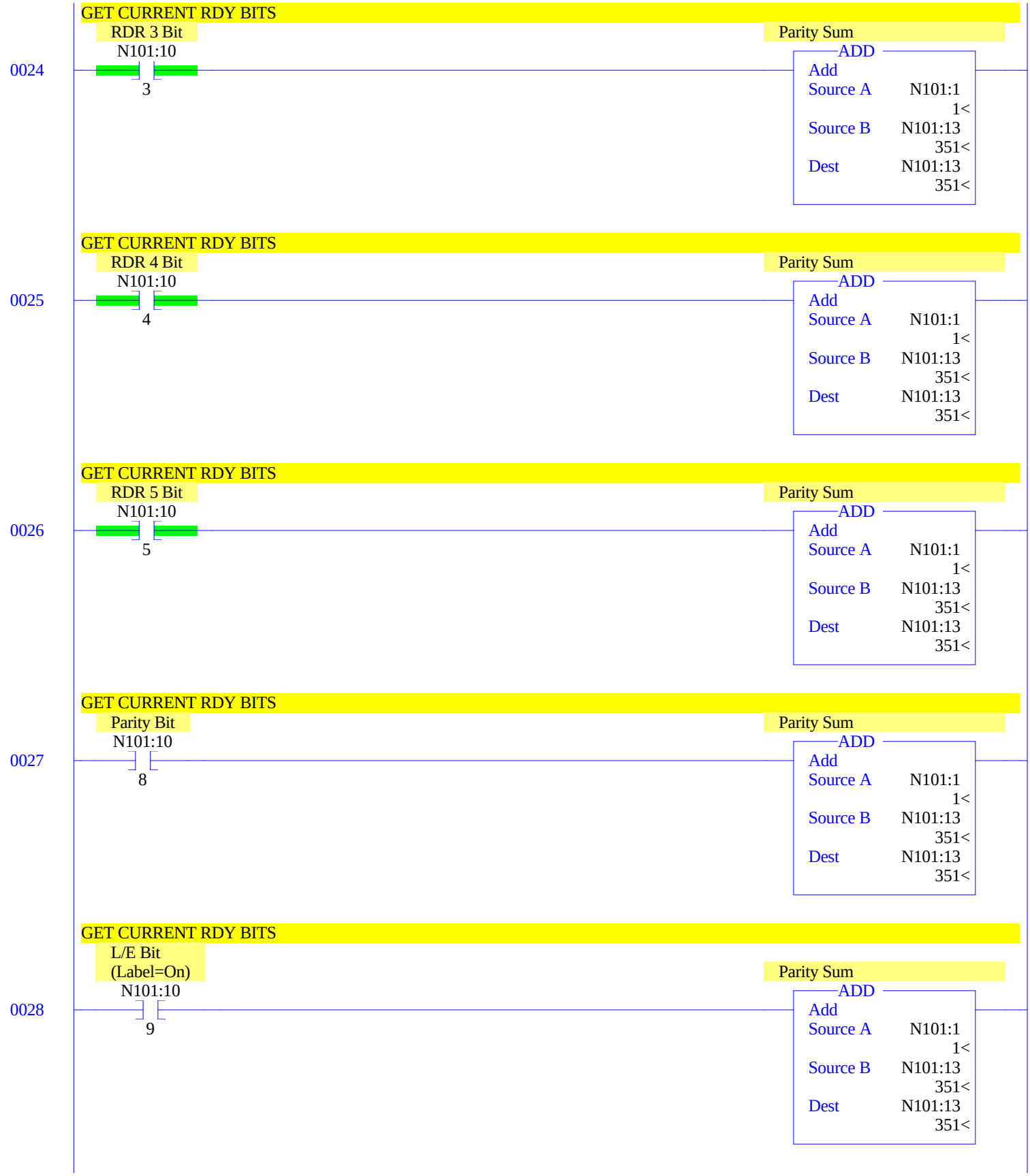

****
Get the current RDY bits
****
First scan of ladder or SFC step
S:1
15
0000
MOV
Move
Source
I:000
76<
Dest
N101:10
63<
****
Is new data available? Check to see if the RDY bits have changed state and make sure that the RDY bits are not both in the same state.
****
First scan of ladder or SFC step
S:1
15
RDY 0
N101:10
6
Last State ACK 0
N101:14
0
RDY 1
N101:10
7
New Data Available Bit
N101:12
0
0001
RDY 1
N101:10
7
Last State ACK 1
N101:14
1
RDY 0
N101:10
6
New Data Available Bit
N101:12
0
0002
Q2:0
JMP
****
Get the Data Bits (D0 - D16)
****
Data Bits (D0 - D16)
0003
MOV
Move
Source
I:001
439<
Dest
N101:11
1<

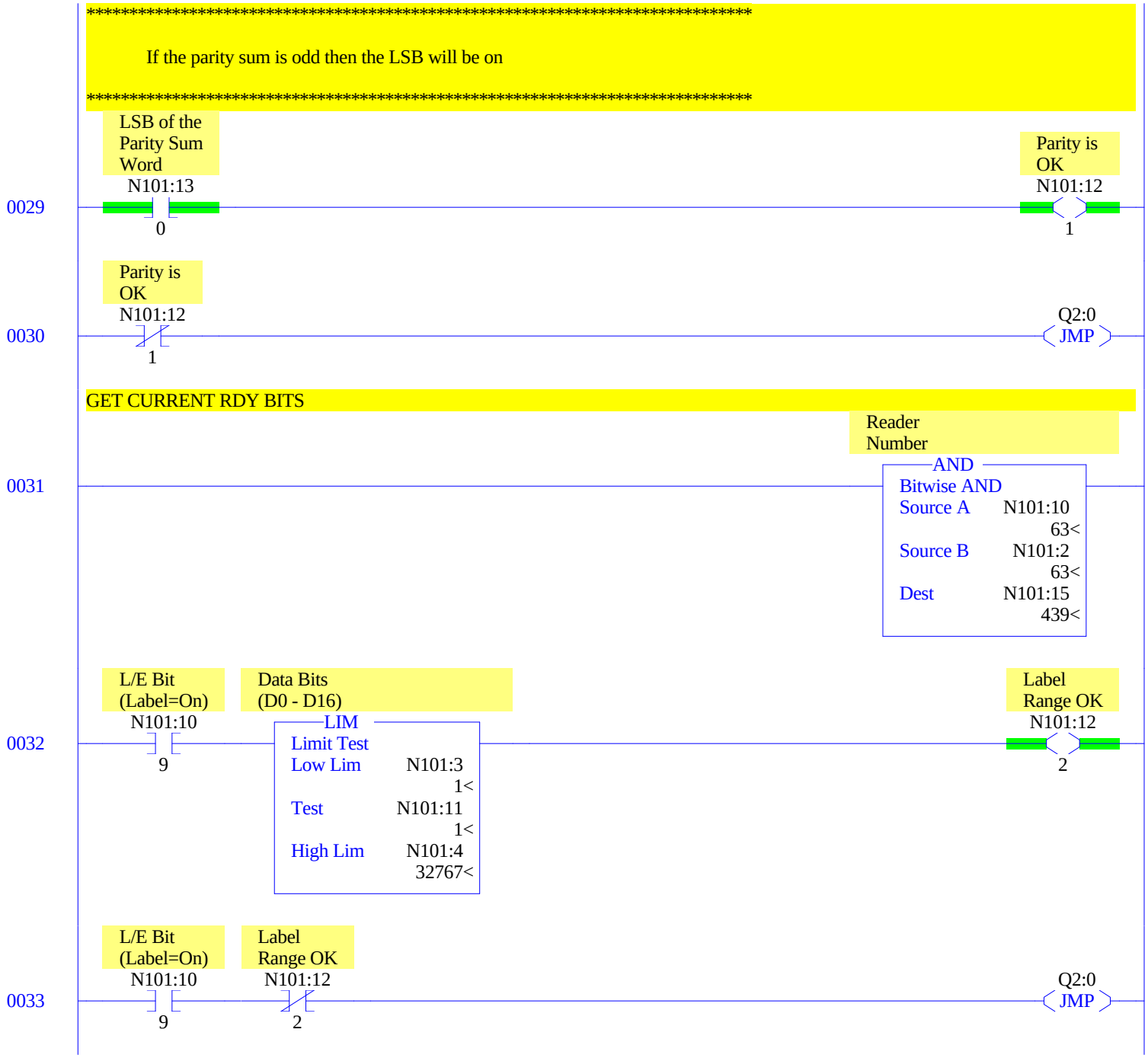

GET CURRENT RDY BITS
Parity Sum
0004
CLR
Clear
Dest N101:13
351<
GET CURRENT RDY BITS
D0 Bit
N101:11
0
Parity Sum
0005
ADD
Add
Source A N101:1
1<
Source B N101:13
351<
Dest N101:13
351<
GET CURRENT RDY BITS
D1 Bit
N101:11
1
Parity Sum
0006
ADD
Add
Source A N101:1
1<
Source B N101:13
351<
Dest N101:13
351<
GET CURRENT RDY BITS
D2 Bit
N101:11
2
Parity Sum
0007
ADD
Add
Source A N101:1
1<
Source B N101:13
351<
Dest N101:13
351<
GET CURRENT RDY BITS
D3 Bit
N101:11
3
Parity Sum
0008
ADD
Add
Source A N101:1
1<
Source B N101:13
351<
Dest N101:13
351<

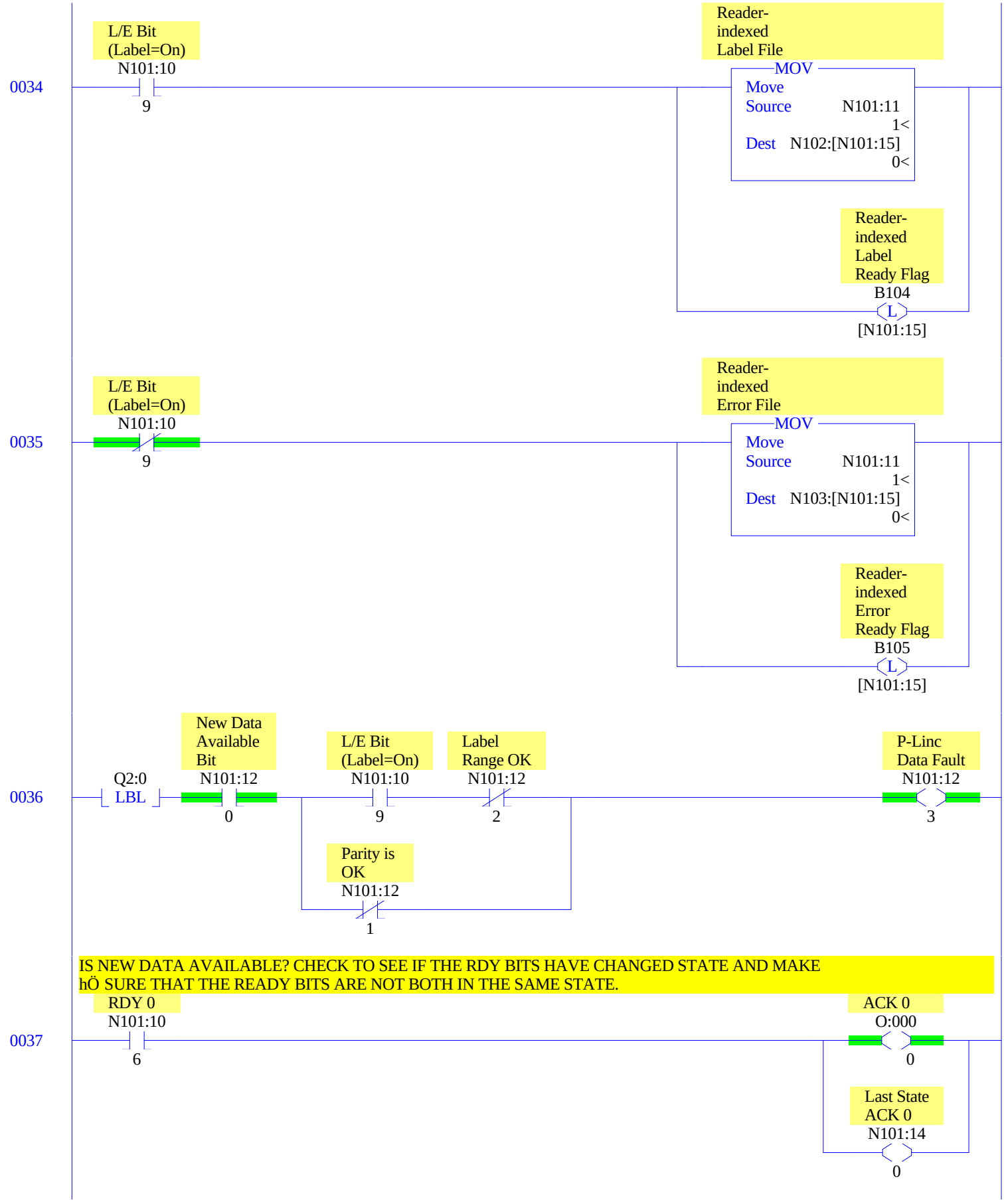

GET CURRENT RDY BITS
D4 Bit
N101:11
4
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0009
GET CURRENT RDY BITS
D5 Bit
N101:11
5
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0010
GET CURRENT RDY BITS
D6 Bit
N101:11
6
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0011
GET CURRENT RDY BITS
D7 Bit
N101:11
7
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0012
GET CURRENT RDY BITS
D8 Bit
N101:11
8
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0013

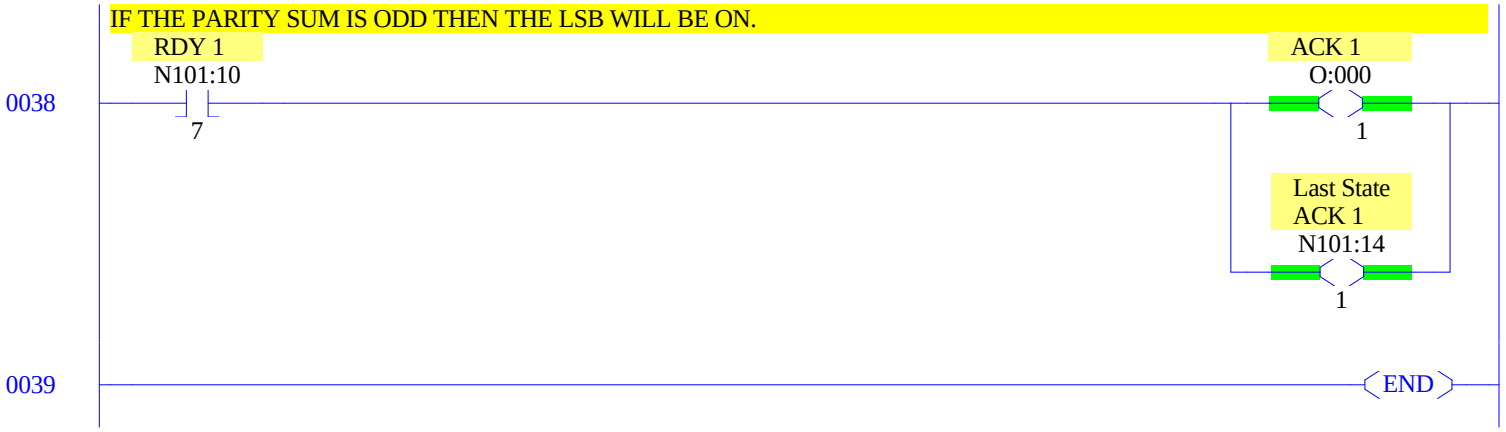

GET CURRENT RDY BITS
D9 Bit
N101:11
9
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0014
GET CURRENT RDY BITS
D10 Bit
N101:11
10
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0015
GET CURRENT RDY BITS
D11 Bit
N101:11
11
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0016
GET CURRENT RDY BITS
D12 Bit
N101:11
12
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0017
GET CURRENT RDY BITS
D13 Bit
N101:11
13
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0018


GET CURRENT RDY BITS
D14 Bit
N101:11
14
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0019
GET CURRENT RDY BITS
D15 Bit
N101:11
15
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0020
GET CURRENT RDY BITS
RDR 0 Bit
N101:10
0
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0021
GET CURRENT RDY BITS
RDR 1 Bit
N101:10
1
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0022
GET CURRENT RDY BITS
RDR 2 Bit
N101:10
2
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
0023


GET CURRENT RDY BITS
RDR 3 Bit
N101:10
3
0024
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
GET CURRENT RDY BITS
RDR 4 Bit
N101:10
4
0025
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
GET CURRENT RDY BITS
RDR 5 Bit
N101:10
5
0026
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
GET CURRENT RDY BITS
Parity Bit
N101:10
8
0027
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<
GET CURRENT RDY BITS
L/E Bit
(Label=On)
N101:10
9
0028
Parity Sum
ADD
Add
Source A N101:1 1<
Source B N101:13 351<
Dest N101:13 351<


****
If the parity sum is odd then the LSB will be on
****
LSB of the Parity Sum Word
N101:13
0
Parity is OK
N101:12
1
0029
Parity is OK
N101:12
1
Q2:0
JMP
0030
GET CURRENT RDY BITS
Reader Number
AND
Bitwise AND
Source A N101:10 63<
Source B N101:2 63<
Dest N101:15 439<
0031
L/E Bit (Label=On)
N101:10
9
Data Bits (D0 - D16)
LIM
Limit Test
Low Lim N101:3 1<
Test N101:11 1<
High Lim N101:4 32767<
Label Range OK
N101:12
2
0032
L/E Bit (Label=On)
N101:10
9
Label Range OK
N101:12
2
Q2:0
JMP
0033


0034
L/E Bit (Label=On)
N101:10
9
Reader-indexed Label File
MOV
Move
Source N101:11
1<
Dest N102:[N101:15]
0<
Reader-indexed Label Ready Flag
B104
L
[N101:15]
0035
L/E Bit (Label=On)
N101:10
9
Reader-indexed Error File
MOV
Move
Source N101:11
1<
Dest N103:[N101:15]
0<
Reader-indexed Error Ready Flag
B105
L
[N101:15]
0036
Q2:0
LBL
New Data Available Bit
N101:12
0
L/E Bit (Label=On)
N101:10
9
Label Range OK
N101:12
2
P-Linc Data Fault
N101:12
3
Parity is OK
N101:12
1
IS NEW DATA AVAILABLE? CHECK TO SEE IF THE RDY BITS HAVE CHANGED STATE AND MAKE
hÖ SURE THAT THE READY BITS ARE NOT BOTH IN THE SAME STATE.
0037
RDY 0
N101:10
6
ACK 0
O:000
0
Last State ACK 0
N101:14
0


IF THE PARITY SUM IS ODD THEN THE LSB WILL BE ON.
RDY 1
N101:10
7
ACK 1
O:000
1
Last State
ACK 1
N101:14
1
0038
0039
END